WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device, comprising:

a nonvolatile memory cell array having a one-time programming region accessed in response to a first decoding signal and a normal region accessed in response to a second decoding signal, wherein the nonvolatile memory cell array performs a read operation and a write operation;

a data write circuit writing data in the nonvolatile memory cell array in response to a write enable signal during the write operation;

a data read circuit reading data output from the nonvolatile memory cell array in response to a sense amplifier enable signal during the read operation; and

a controller for activating the sense amplifier enable signal when the first decoding signal is generated and comparing data output from the data read circuit to generate the write enable signal during the write operation.

2. The device of claim 1, wherein new data is rewritten to the nonvolatile memory cell array without performing an erase operation.

3. The device of claim 1, wherein the controller comprises:

a program detecting circuit comparing data output from the data read circuit in response to a control signal to generate a comparison detecting signal; and

a control means for (a) inactivating the control signal when a specific mode signal is activated, (b) activating the control signal and the sense amplifier enable signal when the specific mode signal is inactivated and the first decoding signal is generated, and (c) activating the write enable signal when the comparison detecting signal is activated during the write operation.

4. The device of claim 3, wherein the control means activates the sense amplifier enable signal during the read operation.

5. The device of claim 3, wherein the program detecting circuit is enabled when the control signal is activated and is disabled when the control signal is inactivated, wherein when the control signal is activated, the comparison detecting signal is activated if data output from the data read circuit are all "0" (or "1").

6. The device of claim 1, wherein the one-time programming region is programmed with certain data.

7. A nonvolatile semiconductor memory device, comprising:

a nonvolatile memory cell array which has a one-time programming region and a parity bit region accessed in response to a first decoding signal and a normal region accessed in response to a second decoding signal, wherein the nonvolatile memory cell array performs a read operation and a write operation;

a data write circuit writing data in the nonvolatile memory cell array in response to a write enable signal during the write operation;

a data read circuit reading data output from the nonvolatile memory cell array in response to a sense amplifier enable signal during the read operation; and

a controller for, during the write operation, (a) activating the sense amplifier enable signal when the first decoding signal is generated, (b) comparing data of the parity bit region output from the data read circuit to generate a first comparison detecting signal, (c) comparing data of the one-time programming region output from the data read circuit to generate a second comparison detecting signal in response to a second comparison detecting signal, and (d) generating the write enable signal in response the first and second comparison detecting signals.

8. The device of claim 7, wherein new data is rewritten to the nonvolatile memory cell array without performing an erase operation.

9. The device of claim 7, wherein the data of the one-time programming region is read synchronously as the data of the parity bit region is output.

10. The device of claim 7, wherein the controller comprises:

a first program detecting circuit enabled in response to a first control signal to compare data of the parity bit region output from the data read circuit to thereby generate the first comparison detecting signal;

a second program detecting circuit enabled in response to a second cotnrol signal to compare data output from the data read circuit to thereby generate the second comaprison detecting signal; and

a controller for, during the write operation, (a) inactivating the first and second control signals when a specific mode signal is activated, (b) activating the first and second control signals and the sense amplifier enable signal when the specific mode signal is inactivated and the first decoding signal is generated, and (c) activating the write enable signal when the first and second comparison detecting signals are activated.

11. The device of claim 10, wherein when the specific mode signal is inactivated, the controller (a) activates the first control signal and the sense amplifier enable signal when the first decoding signal is generated, (b) activates the second control signal when the first comparison detecting signal is activated, and (c) activates the write enable signal when the second comparison detecting signal is activated.

12. The device of claim 10, wherein the control means activates the sense amplifier enable signal during the read operation.

13. The device of claim 10, wherein the first program detecting circuit is enabled when the first control signal is activated and is disabled when the first control signal is inactivated, wherein when the first control signal is activated, the first comparison detecting signal is activated if data output from the data read circuit are all "0" (or "1).

14. The device of claim 10, wherein the second program detecting circuit is enabled when the second control signal is activated and is disabled when the second control signal is inactivated, wherein when the second control signal is activated, the second comparison detecting signal is activated if data output from the data read circuit are all "0" (or "1").

15. The device of claim 7, wherein the one-time programming region is programmed with certain data.

16. The device of claim 7, wherein the parity bit region is programmed with parity data, the parity data representing that the one-time programming region is programmed with certain data.

17. The device of claim 16, wherein the parity data comprises a single bit "0" or 1".

18. A one-time programming control method of a nonvolatile semiconductor memory device having a nonvolatile memory cell array which is divided into a one-time programming region and a normal region, wherein the nonvolatile semiconductor memory device performs a read operation and a write operation, the method comprising:

determining whether the one-time programming region is accessed during the write operation;

comparing data read from the one-time programming region to generate a comparison detecting signal when the one-time programming region is accessed;

stopping the write operation when the comparison detecting signal is not activated; and

writing data in the one-time programming region when the one-time programming region is not accessed or the comparison detecting signal is activated.

19. The method of claim 18, wherein new data is rewritten to the nonvolatile memory cell array without performing an erase operation.

20. The method of claim 18, wherein the one-time programming region is all programmed with certain data.

21. A one-time programming control method of a nonvolatile semiconductor memory device having a nonvolatile memory cell array which is divided into a one-time programming region, a parity bit region and a normal region, wherein the nonvolatile semiconductor memory device performs a read operation and a write operation, the method comprising:

determining whether the one-time programming region is accessed during the write operation;

comparing data read from the parity bit region to generate a first comparison detecting signal when the one-time programming region and the parity bit region are accessed, and comparing data read from the one-time programming region to generate a second comparison detecting signal when the first comparison detecting signal is generated;

stopping the write operation when the first or the second comparison detecting signal is not activated; and

writing data in the one-time programming region when the one-time programming region and the parity bit region are not accessed or the second comparison detecting signal is activated.

22. The method of claim 21, wherein new data is rewritten to the nonvolatile memory cell array without performing an erase operation.

23. The method of claim 21, wherein the one-time programming region is all programmed with certain data.